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Notice of Allowability	Application No.	Applicant(s)	
	10/739,202	PARK, GEON-OOK	
	Examiner	Art Unit	
	Evan Pert	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the application filed December 19, 2003*.

2. ☒ The allowed claim(s) is/are *1-10*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 1203
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Note: This application has been amended merely to clarify and place the application in better form for a higher quality patent (i.e. the examiner's amendment does not alter the intended scope of the originally filed claims, but rather clarifies and corrects trivial informalities such as typographical errors and improper idiomatic English).

The application has been amended as follows:

- **Replace** the originally filed **claims 1-10** with the following claims:

[continued]

1. A method of forming a gate electrode in a semiconductor device, comprising the steps of:

forming a gate oxide on a semiconductor substrate;

depositing polysilicon on the gate oxide;

forming a mask formation film on the polysilicon;

patterning the mask formation film twice, using a photolithography process for each patterning, wherein one photolithography process is performed with a mask pattern which masks neighboring gate electrode areas and an area between the neighboring gate electrode areas, and the other photolithography process is performed with a mask pattern which exposes the area between the neighboring gate electrode areas;

etching the polysilicon using the patterned mask formation film; and

removing mask formation film remaining on the polysilicon.

2. The method of claim 1, wherein the mask formation film is patterned by a photolithography process with a mask pattern which masks neighboring gate electrode areas and the area between the neighboring gate electrode areas, and then by a photolithography process with a mask pattern which exposes the area between the neighboring gate electrode areas.

3. The method of claim 1, wherein the mask film is patterned by a photolithography process with a mask pattern which exposes the area between the neighboring gate electrode areas, and then by a photolithography process with a mask pattern which masks neighboring gate electrode areas and the area between neighboring gate electrode areas.

4. The method of claim 1, wherein the mask thin film is made from material having a great di#erence in etching rate from the polysilicon.

5. The method of claim 4, wherein the mask thin film is silicon oxynitride or silicon nitride.

[continued]

6. A method of forming a gate electrode in a semiconductor device, comprising the steps of:

forming a gate oxide on a silicon substrate;

depositing polysilicon to function as a gate electrode on the gate oxide, and then forming a mask formation film to be used as a mask when the gate electrode is etched from the polysilicon,

forming a first pattern of photoresist on the mask formation film, and then performing a first etching step of etching the mask formation film based on the first pattern of photoresist;

removing the first pattern of photoresist;

forming a second pattern of photoresist on a portion of the mask formation film remaining after the first etching step and on the polysilicon, and then performing a second etching step of etching the mask formation film based on the second pattern of photoresist;

removing the second pattern of photoresist, and then etching the polysilicon using the mask thin film partially remaining on the polysilicon; and

forming the gate electrode by removing the mask formation film remaining on the polysilicon.

7. The method of claim 6, wherein the mask formation film is made from material having a great difference in etching rate from the polysilicon.

8. The method of claim 1 or 7, wherein the mask formation film is a film of silicon oxynitride or silicon nitride deposited by a PECVD method.

9. The method of claim 6, wherein the etching of the mask formation film in the first and second etching steps is performed until the polysilicon is exposed.

10. The method of claim 6, wherein, in the step of forming the gate electrode, the mask formation film is removed by a wet etching.

[continued]

- Change the title to:

--Formation method of a gate electrode in a semiconductor process--.

- Enter the following changes in the specification:
- At p. 1, lines 12-17, replace the entire paragraph with:

--With the development of manufacturing techniques for semiconductor devices and the expansion of their applications, research and development into increased integration of semiconductor devices has progressed rapidly. Also, with the increased integration of semiconductor devices, studies for downsizing semiconductors based on microscopic process technologies have progressed.--.

- At p. 1, line 18, change "downsizing of the semiconductor device" to –downsizing of semiconductor devices--.
- At p. 1, line 34, after "to be formed" insert –(i.e. gate electrode 10 not yet patterned as depicted in Fig. 1)--.
- At p. 2, line 2, change "is various" to –includes multiple wavelengths of differing lengths,--.
- At p. 2, line 12, change "face with" to –faced with--.
- At p. 2, line 16, change "considerations" to –consideration--.
- At p. 2, line 17, change "to a method" to –to provide a method--.
- At p. 2, line 25, change "a mask thin film" to --thin mask formation film--.
- At p. 2, line 25, change "the mask thin film" to –the mask formation film--.
- At p. 2, line 31, change "the mask thin film" to –the mask formation film--.

[continued]

- At p. 3, line 22, change "a curing mask" to –the mask—
- At p. 3, line 22, change "through a" to --by a--.
- At p. 3, line 26, change "mask thin film 14" to –mask formation film 14--.
- At p. 3, line 26, change "a curing mask" to –a gate etching mask--.
- At p. 3, line 27, change "electrode is etched later is formed" to –gate electrode is etched from the polysilicon after patterning the mask formation film--.
- At p. 3, line 28, change "the mask thin film 14" to –the mask formation film 14--.
- At p. 3, line 28, change "preferable to use" to –preferably a--.
- At p. 3, line 23, change "the mask thin film 14" to –the mask formation film 14--.

Allowable Subject Matter

2. Claims 1-10 are allowed.

3. The following is an examiner's statement of reasons for allowance:

The prior art certainly discloses methodology of forming a gate electrode in a semiconductor device (e.g. gate electrodes having sub-lithographic gate electrode widths), yet the prior art does not disclose applicant's claimed method that includes two patterning steps of a (i.e. the same) mask formation film (e.g. SiON) to form a mask for etching a narrow gate electrode.

The two distinct steps of patterning (i.e. the first photolithographic patterning and etching followed by the second photolithographic patterning and etching) of the mask formation film are necessarily "formed in a partially overlapped manner with a difference in time" which can result in an "ultramicroscopic line width" in the "overlapped region" which is advantageous [e.g. see p. 4, line 32 to p. 5, line 4].

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EVAN PERT
PRIMARY EXAMINER

ETP
September 18, 2005